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EXAMINER	
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ART UNIT	**PAPER NUMBER**
2133	7

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/976,731	SONG, LEILEI
	Examiner	Art Unit
	Joseph D. Torres	2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) *11-24 and 27* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,7-10,25 and 26* is/are rejected.

7)☒ Claim(s) *4-6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Group I, Claims 1-10, 25 and 26 in Paper No. 6 is acknowledged. The traversal is on the ground(s) that the search only requires searching three subclasses within a single class. This is not found persuasive because the three subclasses cited in the previous Office Action are only the classes where the different invention should be classified. A complete search for Group I must include class 714, subclasses 704, 708, 781, 782, 784, 785; class 375, subclass 225; class 341, subclass 94; and class 340, subclass 7.32 comprising 3295 patents that must be searched for specific language. In addition, the Examiner would like to point out that it has not only take the Examiner one search for the current group but an additional in the current office action to find the appropriate arts to reject claims form Group I. The Examiner asserts that a proper examination of Groups II and III would require additional and equally extensive searches due to the complexity and differences of the current claim language.

The requirement is still deemed proper and is therefore made FINAL.

Claims 11-24 and 27 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected inventions, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in Paper No. 6.

Drawings

2. In view of the corrections to the drawings in Amendment A of Paper No. 6, the Examiner withdraws all objections to the drawings.

Claim Rejections - 35 USC § 112

3. In view of the corrections to claims 4-6 in Amendment A of Paper No. 6, the Examiner withdraws all previous 35 USC § 112 rejections in the last Office Action to claims 4-6.

Response to Arguments

4. Applicant's arguments with respect to claims 1-3, 7-10, 25 and 26 have been considered but are moot in view of the new ground(s) of rejection.

Examiner's Comment.

MPEP § 2131.01 states "To serve as an anticipation when the reference is silent about the asserted inherent characteristic, such gap in the reference may be filled with recourse to extrinsic evidence. Such evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." Continental Can Co. USA v. Monsanto Co., 948 F.2d 1264, 1268, 20 USPQ2d 1746, 1749 (Fed. Cir. 1991). The Examiner introduces Ott, Stefan (US 6182264 B1) and Wasada, Langford M. (US 5970075 A) as teaching references for that which is inherent in the Yang patent. More

specifically Yang teaches an iterative algorithm comprising various processing steps and Ott teaches unnecessary error correction wastes processor capacity in the receiving and transmitting devices and signal processing effort is wasted encoding and decoding error correction information, which in turn, needlessly slows the performance of the system and increases power consumption (col. 2, lines 10-13, Ott), that is, decreased error correction processing reduces power consumption just as increased error correction processing increases power consumption. In addition, Yang teaches the use of identification of uncorrectable errors for Reed-Solomon codes (see Abstract, Yang) and Wasada teaches the well-known relationship between uncorrectable errors and the error location polynomial, that is; if the degree of the error locator polynomial is greater than the maximum number of correctable errors for a Reed-Solomon block of code, then the block is uncorrectable (col. 9, lines 29-33, Wasada).

Claim Rejections - 35 USC § 102

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 7-10, 25 and 26 are rejected under 35 U.S.C. 102(e) as being anticipated by Stevenson; Carl R. (US 6209112 B1).

35 U.S.C. 102(e) rejection of claims 1, 25 and 26.

Stevenson teaches determining if an actual number of errors is less than a maximum error correction capability; and reducing power consumption in a decoder of the error correction system when the actual number of errors is less than the maximum error correction capability (col. 2, lines 28-32 in Stevenson teaches that if no error correction is required, then error-correction circuitry is disabled; claim 1 teaches that the means for determining if error correction is required is carried out by comparing checksums whereby if the checksums are equal, then error correction is not required; Note: if the checksums are equal then an actual number of errors is less than a maximum error correction capability hence Stevenson teaches determining if an actual number of errors is less than a maximum error correction capability by comparing checksums and reducing power consumption in a decoder of the error correction system by disabling the decoder when the actual number of errors is less than the maximum error correction capability).

35 U.S.C. 102(e) rejection of claims 7 and 8.

See rejection to claim 1 and 25, above. Note: Syndromes are defined as the difference between checksums and if the checksums are equal, then the syndromes are all equal to zero.

35 U.S.C. 102(e) rejection of claim 9.

Col. 4, lines 11-14 in Stevenson teaches the use of Reed-Solomon codes. Reed Solomon decoders inherently include syndrome generators and key equation solver

suing the syndromes during the error correction process. If the decoder is disabled then so is the key equation-solving device within the decoder.

35 U.S.C. 102(e) rejection of claim 10.

If the Syndromes are not all zero in Stevenson the error correction circuitry is enabled to correct errors (see rejection to Claim 1, above). Calculating error polynomials is a required step for decoding Reed-Solomon codes (Col. 4, lines 11-14 in Stevenson).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stevenson; Carl R. (US 6209112 B1) in view of the Applicant's Admitted Prior Art.

35 U.S.C. 103(a) rejection of claim 2.

Stevenson, substantially teaches the claimed invention described in claims 1 and 25 (as rejected above).

However Stevenson, does not explicitly teach the specific use of gating clocks.

The Applicant admits in lines 26 and 27 of page 15 that clock gating is a well known in the art. The Examiner asserts that Stevenson teaches reducing power consumption of error decoding circuitry when errors are less then a maximum error correction capability. It would be an obvious Engineering design choice to use a circuit technique well-know in the art based on available circuitry and available circuit techniques for carrying out the circuit design requirements.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Stevenson with the teachings of Applicant's Admitted Prior Art by including use of gating clocks. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of gating clocks would have provided the opportunity to implement control circuitry for the method taught in the Stevenson patent whereby power consumption of error decoding circuitry is reduced when errors are less then a maximum error correction capability.

7. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stevenson; Carl R. (US 6209112 B1) in view of Yang, Honda et al. (US 6606727 B1, hereafter referred to as Yang).

35 U.S.C. 103(a) rejection of claim 3.

Stevenson, substantially teaches the claimed invention described in claims 1 and 25 (as rejected above).

However Stevenson, does not explicitly teach the specific use of a step for **determining if a degree of at least one of the intermediate polynomials is less than a predetermined degree** for use in detecting an uncorrectable error.

The Examiner asserts that that Yang teaches, in Step 67 in Figure 5 of Yang, decoding is completed and after Step 67 a test for uncorrectable errors is performed and if it is determined that no uncorrectable errors exist, the processing is terminated (see col. 8, lines 45-46; Note: an uncorrectable error is an error that exceeds the maximum error correction capability of an error correction code; hence processing in Figure 5 of Yang is stopped if it is determined that an actual number of errors is less than a maximum error correction capability). The Examiner asserts that it is well-known in the art that if the degree of the error locator polynomial is greater than the maximum number of correctable errors for a Reed-Solomon block of code, then the block is uncorrectable (see above Examiner's Comment regarding the Wasada reference; Note: an error locator polynomial is an intermediate polynomial since it is only used in intermediate steps for error correction and is not a final result); hence if the degree of the error locator polynomial is less than the maximum number of correctable errors the block is correctable. Therefore it would be obvious to use that which is well-known in the art for

determining an uncorrectable error to carry out the required step in the Yang patent of determining whether a block of Reed-Solomon code is correctable or not.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings in the Stevenson patent with the teachings in the Yang patent by including an additional step of for determining if a degree of at least one of the intermediate polynomials is less than a predetermined degree. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that for determining if a degree of at least one of the intermediate polynomials is less than a predetermined degree would have provided the opportunity to carry out the required step in the Yang patent of determining whether a block of Reed-Solomon code is correctable or not (see col. 8, lines 45-46 in Yang).

Allowable Subject Matter

8. Claim 4-6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an Examiner's statement of reasons for the indication of allowable subject matter:

The present invention pertains to amethod performed in an error correction system, the method comprising the steps of: determining if an actual number of errors is less than a

maximum error correction capability; and reducing power consumption in a decoder of the error correction system when the actual number of errors is less than the maximum error correction capability.

Claim 4 recites various features:

"wherein one intermediate polynomial is a first error evaluator polynomial R(x), wherein one intermediate polynomial is a first error locator polynomial F(x), wherein $R^{(r+1)}(x) = F^{(r+1)}(x)S(x) \bmod x^{2t}$ wherein r is a number of iterations, S(x) is a syndrome polynomial and t is a number of errors capable of being corrected, wherein one intermediate polynomial is a second error evaluator polynomial Q(x), wherein one intermediate polynomial is a second error locator polynomial G(x), wherein $Q^{(r+1)}(x) = G^{(r+1)}(x)S(x) \bmod x^{2t}$ and wherein the step of determining if a degree of at least one of the intermediate polynomials is less than a predetermined degree further comprises the step of determining if a degree of either R(x) or Q(x) is less than a predetermined degree, wherein R(x) and F(x) rare valid when a degree of R(x) is less than the predetermined degree, and wherein Q(x) and G(x) are valid when a degree of Q(x) is less than the predetermined degree".

The Prior Art of record and in particular Stevenson (US 6209112 B1) teach determining if an actual number of errors is less than a maximum error correction capability; and reducing power consumption in a decoder of the error correction system when the actual number of errors is less than the maximum error correction capability (col. 2, lines 28-32 in Stevenson teaches that if no error correction is required, then error-correction circuitry is disabled; claim 1 teaches that the means for determining if error

correction is required is carried out by comparing checksums whereby if the checksums are equal, then error correction is not required; Note: if the checksums are equal then an actual number of errors is less than a maximum error correction capability hence Stevenson teaches determining if an actual number of errors is less than a maximum error correction capability by comparing checksums and reducing power consumption in a decoder of the error correction system by disabling the decoder when the actual number of errors is less than the maximum error correction capability).

The prior art however are not concerned with and do not teach, suggest, or otherwise render obvious the step of determining if a degree of at least one of the intermediate polynomials is less than a predetermined degree further comprises the step of determining if a degree of either R(x) or Q(x) is less than a predetermined degree, wherein R(x) and F(x) rare valid when a degree of R(x) is less than the predetermined degree, and wherein Q(x) and G(x) are valid when a degree of Q(x) is less than the predetermined degree wherein one intermediate polynomial is a first error evaluator polynomial R(x), wherein one intermediate polynomial is a first error locator polynomial F(x), wherein $R^{(r+1)}(x) = F^{(r+1)}(x)S(x) \bmod x^{2t}$, wherein r is a number of iterations, S(x) is a syndrome polynomial and t is a number of errors capable of being corrected, wherein one intermediate polynomial is a second error evaluator polynomial Q(x), wherein one intermediate polynomial is a second error locator polynomial G(x), wherein $Q^{(r+1)}(x) = G^{(r+1)}(x)S(x) \bmod x^{2t}$ as taught by claim 4 and its base and intervening claims. Hence the prior art taken alone or in any combination fail to teach the claimed novel feature in claim 4 in view of its base and intervening claims.

Claim 5 recites various features:

"the step of providing, in the decoder, a plurality of intermediate polynomial elements and a calculation circuit coupled to the intermediate polynomial elements, each intermediate polynomial element containing coefficients of one of the intermediate polynomials, and wherein the step of reducing power consumption in a decoder of the error correction system when the actual number of errors is less than the maximum error correction capability further comprises the step of placing a predetermined state into each of the intermediate polynomials polynomial elements, the predetermined state selected to reduce switching of the calculation circuit".

The prior art however are not concerned with and do not teach, suggest, or otherwise render obvious the step of providing, in the decoder, a plurality of intermediate polynomial elements and a calculation circuit coupled to the intermediate polynomial elements, each intermediate polynomial element containing coefficients of one of the intermediate polynomials, and wherein the step of reducing power consumption in a decoder of the error correction system when the actual number of errors is less than the maximum error correction capability further comprises the step of placing a predetermined state into each of the intermediate polynomials polynomial elements, the predetermined state selected to reduce switching of the calculation circuit as taught by claim 5 and its base and intervening claims. Hence the prior art taken alone or in any combination fail to teach the claimed novel feature in claim 5 in view of its base and intervening claims.

Claim 6 depends from claim 5.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Croft; Thomas Milton et al. (US 5701329 A) teaches a method of and apparatus for reducing power consumption of portable radio communication systems, such as mobile telephones, in standby mode to increase the time between necessary battery charges and recharges.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Art Unit 2133